ABSTRACT OF THE DISCLOSURE

Memory integrated circuitry includes an array of memory cells formed over a semiconductive substrate and occupying area thereover, at least some memory cells of the array being formed in lines of active area formed within the semiconductive substrate which are continuous between adjacent memory cells, said adjacent memory cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent memory cells. At least some adjacent lines of continuous active area within the array are isolated from one another by LOCOS field oxide formed therebetween. The respective area consumed by individual of said adjacent memory cells is ideally equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array. The respective area is preferably no greater than about $7F^2$, and most preferably no greater than about $6F^2$.